REMARKS

This amendment responds to the Office Action dated May 7, 2001 in which the Examiner objected to the drawings, rejected claims 1-25 under 35 U.S.C. § 112, first paragraph, rejected claims 1-13 under 35 U.S.C. § 112, second paragraph and rejected claims 1-25 under 35 U.S.C. § 102(e) or in the alternative under 35 U.S.C. § 103.

Claims 1-13 were rejected under 35 U.S.C. § 112, first paragraph as claiming that the operation of the second instruction is executed in both the third and fourth periods. As indicated above, claim 1 has been amended to better indicate that the phrase "in a third period" indicates when the second control signal is output. In particular, in the third period, a control signal is output by decoding a second instruction. In the fourth period, a determination of whether or not the predetermined condition is satisfied and then the operation designated by the second instruction is executed based upon the results of the determination of the predetermined condition. It is therefore respectfully submitted that the claims contain subject matter which is described in the specification in such a way as to enable one skilled in the art to which it pertains, to make and/or use the invention. It is therefore respectfully requested that the Examiner withdraws the rejection to claims 1-13 under 35 U.S.C. § 112, first paragraph.

Claims 1-25 were rejected under 35 U.S.C. § 112, first paragraph. Applicants respectfully traverse the Examiner's statement that "certain capabilities are provided to the invention by the format of the VLIW instruction while other capabilities are provided by the format of the sub-instructions which are critical or essential to the practice of the invention and are not included in the claims". Furthermore, claims 1-13 were rejected

under 35 U.S.C. § 112, second paragraph, and the drawings were objected to for not showing the timing relations. Applicants respectfully traverse. In particular, Figure 8 clearly shows instructions I01, I11, I21, I31, I41, I51 and I61. Furthermore, Figure 9 discloses the timing for these instructions. Also, Figure 2 shows the CD field 403 which corresponds to the field for designating timing. In Figure 9, instruction I01 is decoded at cycle T2. A condition is determined at cycle T7 after several cycles from cycle T2. The operation is executed based on the determination. Similarly, Applicants respectfully bring the Examiner's attention to Figures 10 and 11 which are similarly shown with regard to the timing and the instructions. Applicants also respectfully bring the Examiner's attention to Figure 1 which shows the control signals 11 and 12. It is therefore respectfully submitted that the capabilities provided by the format of the sub-instructions is not critical or essential to the practice of the invention. A condition instruction designates an execution of a predetermined operation when a certain condition is satisfied (execution condition is designated in the CC field 401 shown in Figure 2). The feature of the claimed invention is that the timing of determining a condition can be delayed. See Figure 9, cycle T7 or Figure 11, cycle T6. It is therefore respectfully submitted that the specification is enabling, the claims particularly point out and distinctly claim the subject matter which the Applicants regard as the invention and that the drawings clearly show the timed relationships between the actions claimed and when the actions are performed. It is therefore respectfully requested that the Examiner withdraws the rejection to claims 1-25 under 35 U.S.C. § 112, first paragraph, withdraws the rejection to claims 1-13 under 35 U.S.C. § 112, second paragraph and withdraws the objection to the drawings.

As indicated above, claim 1 has been amended only to correct formal matters. It is respectfully submitted that no substantive changes have been made to claim 1.

Claims 1, 14 and 21 claim a data processing device comprising an instruction decoder and an instruction execution unit. The instruction execution unit determines whether or not a predetermined condition is satisfied in a predetermined timing prior to executing the instruction. The prior art does not show, teach or suggest delaying of a time of determining a condition as claimed in claims 1, 14 and 21.

Claims 1-25 were rejected under 35 U.S.C. §102(e) as being anticipated by, or in the alternate, under 35 U.S.C. § 103 as being unpatentable over *Holmann et al* (U.S. Patent No. 5,815,698).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(e) or under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejections to the claims and allows the claims to issue.

Holmann et al appears to disclose in Fig. 13 a basic format 320 of delayed branch instructions. Delayed branch instruction 320 comprises an opcode 321, a field 322 for designating a delayed value and a field 323 for indicating an offset or an address of a target branch address. (col. 13, lines 54-59) When the instruction decoder 8 in the instruction decode unit 8 recognizes that a decoded instruction is a delayed branch instruction, the instruction decoder unit 2 generates a control signal 11 and transfers it to the memory unit 3. In the memory unit 3, the PC controller 13 stores the decoded instruction into register 13A according to the control signal 11 received from the instruction decoder unit 2.

Accordingly, the register 13A stores information indicating the target of a delayed branch instruction. The PC controller 13 stores a PC value related to the time when the branch instruction will be executed into register 13B. When the value of the program counter (PC) in the microprocessor is equal to the value stored in register 13B, the PC controller 13 executes the branch instruction based on the target branch information stored in register 13A. That is, the value designated by the target branch information stored in register 13A is set into the program counter (PC). As a result, when the address of a fetched instructions is equal to the value stored in register 13B, the instruction at the target of a branch is fetched in the following cycles. (col. 14, lines 26-45, emphasis added)

Thus, *Holmann et al* merely discloses a microprocessor which can execute a delayed jump instruction where the field 322 designates the time for executing the branch instruction (i.e., *Holmann et al.* does not delay the time to determine that the jump condition is satisfied but only delays execution of the branch instructions). Nothing in *Holmann et al* shows, teaches or suggests delaying the timing of the determination of a predetermined condition, as claimed in claims 1, 14 and 21. Rather, *Holmann et al* merely discloses that the execution of the instruction is delayed. *Holmann et al* does not disclose delaying of the timing to determine the condition (i.e., an execution condition is not determined at a designated timing).

Since nothing in *Holmann et al* shows, teaches or suggests (a) decoding an instruction in a second period and determining the execution condition in a fourth period which starts after a certain duration of the second period as claimed in claim 1, (b) a register storing a value representing a timing of starting to determine an execution

condition and an instruction execution unit determining the execution condition in response to an event that the timing is detected based upon the value in the first register, as claimed in claim 14, or (c) a field specifying a timing to start a determination of whether a condition is satisfied as claimed in claim 21, it is respectfully requested that the Examiner withdraws the rejection to claims 1, 14 and 21 under 35 U.S.C. §102(e) or in the alternative under 35 U.S.C. §103.

Claims 2-13, 15-20 and 22-25 depend from claims 1, 14 and 21 and recite additional features. It is respectfully submitted that claims 2-13, 15-20 and 22-25 would not have been anticipated by *Holmann et al* within the meaning of 35 U.S.C. §102(e) or obvious over *Holmann et al.* within the meaning of 35 U.S.C. § 103 at least for the reasons as set forth above and since nothing in the reference shows, teaches or suggests determining an execution condition at the timing designated by a value in a third register as claimed in claim 6. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2-13, 15-20 and 22-25 under 35 U.S.C. §102(e) or in the alternative under 35 U.S.C. § 103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, it is respectfully requested that the Examiner enters this amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the

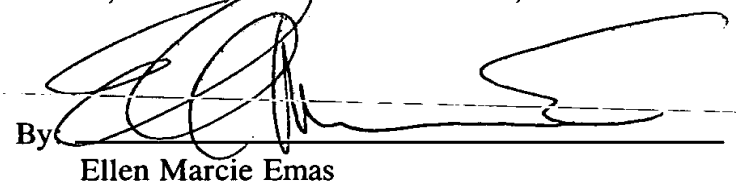
applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.



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Marked-up Claim 1

1. (Twice Amended) A data processing device comprising:

an instruction decoder for sequentially decoding a plurality of instructions described in a program sequence and outputting control signals respectively corresponding to the instructions, and

an instruction execution unit for executing operations respectively designated by said plurality of instructions in accordance with said control signal output from said instruction decoder, wherein

said instruction decoder decodes a first instruction among said plurality of instructions and outputs a first control signal in a first period;

said instruction execution unit executes the operation designated by said first instruction in accordance with said first control signal in a second period succeeding to said first period;

said instruction decoder outputs a second control signal in a third period by decoding a second instruction of which operation is executed under a predetermined condition among said plurality of instructions [in a third period]; and

said instruction execution unit determines whether or not said predetermined condition is satisfied in a fourth period and executes the operation designated by said second instruction in response to a result of the determination, said fourth period being started after elapsing a same time as said second period or longer from an ending of said third period.